PMX1 AGP Reference Card
Design Guide

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Issue 1	23/01/98	First Draft Issue
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1. INTRODUCTION

This document is a design guide for the PMX1 reference card (NLX AGP version).

1.1 Board Features

The PMX1 AGP card has the following main features:-

- NLX form factor AGP card design (AGP v1.0 compliant).
- 8MB SDRAM (100Mhz) graphics memory (also 16MB development only option).
- TV out option (H/W selectable between S-Video or composite video).
- VMI port providing option for video decoder or MPEG-2 daughter-card.

2. TECHNICAL DESCRIPTION

This section is a sheet-by-sheet guide to the PMX1 AGP reference card schematics (issue 20/01/98). These schematics consist of 10 sheets.

2.1 Sheet 1 - Top Level

This shows the main functional blocks similar to that shown in fig 1.1 below.

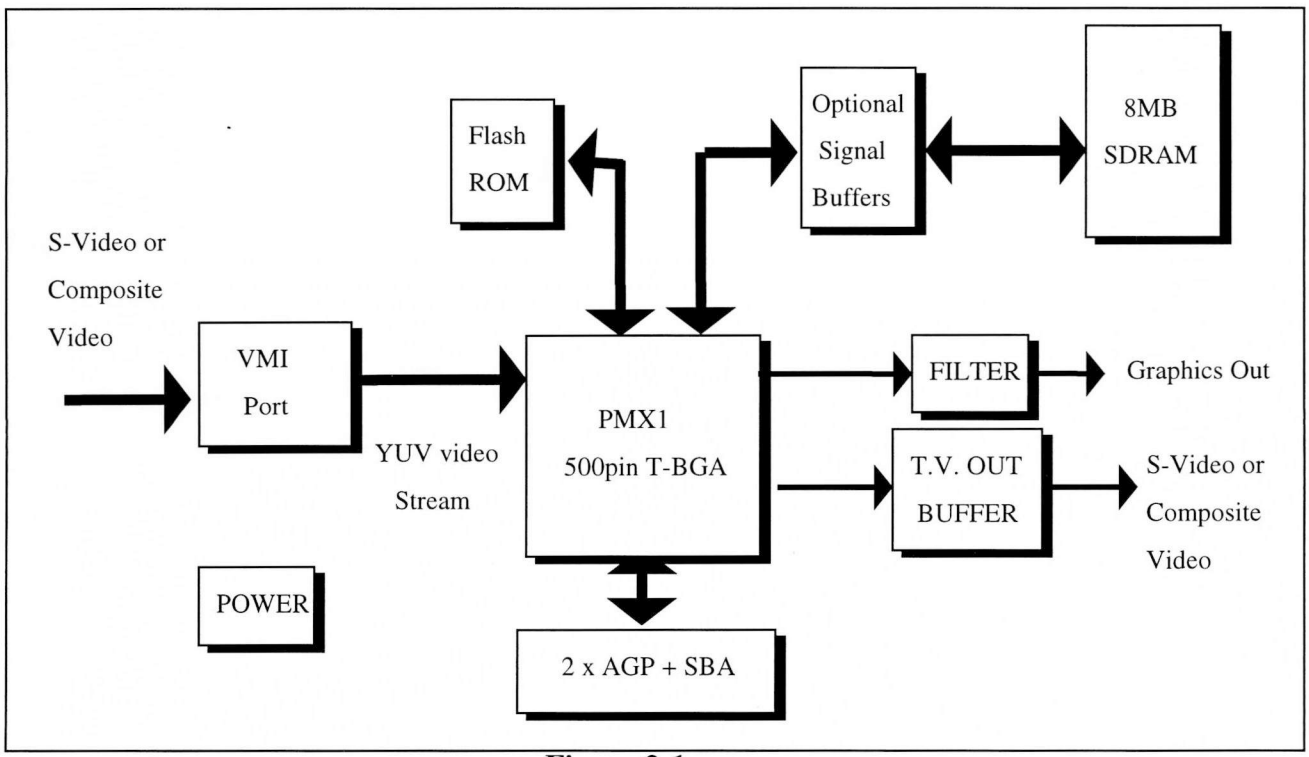


Figure 2-1

2.2 Sheet 2 - AGP Bus Interface

The AGP bus interface is designed to comply with the AGP bus v1.0 specification.

PMX1 supports 2 x AGP (with sideband addressing) mode.

Appendix A shows the pin-out of the AGP/PCI bus connector.

2.3 Sheet 3 - Flash ROM

PMX1 has a 3.3v ROM interface. A Flash ROM is used to enable support for the in-circuit re-programmable BIOS. The graphics card BIOS requires 64KB of memory.

PMX1 does support smaller OTP EPROM devices (e.g. 256/512Kbit), however this card design does not support these devices.

2.4 Sheet 4 - VMI Port

The 40-way header (CN3) is the VMI host port connector. The pin-out for this header is listed in Appendix B. The 26-way header (CN5) is the VMI video port (feature connector) as per VMI v1.4. The pin-out of this header is listed in Appendix C.

S-Video or composite video can be fed from a 4-pin miniDIN connector, which is mounted on a separate card attached to the rear of the main board, through the video-in header CN2, and then via the VMI port to a daughter card containing a video decoder (e.g. Brooktree Bt829A) or MPEG-2 decoder. Bt829A output enable can be controlled by pull-up/pull-down resistor pair (R24/25).

A digitised YUV data stream is supplied back to the PMX1 chip from the video decoder via an 8-bit data bus across the VMI port. A signal buffer (U5) is required to convert the 5V signals of the Bt829A to 3.3V required by the PMX input buffers.

(Note: U5 will not be required when the 3.3V Bt829B device becomes available.

2.5 Sheet 5 - PMX1 Device

PMX1 is packaged in a 500-pin Tape Ball Grid Array (T-BGA) device (U10). The PMX1 Preliminary Data Sheet lists pin-out data and electrical specifications.

2.5.1 PMX1 clocks

PMX1 has the following clock requirements:-

- A 14.31818Mhz crystal (X2) drives **REFCLK**.
- **REFCLK** drives the internal PLL's for **DAC_CLK** (25-220Mhz) & **CORECLK**.
- **CORECLK** generates **SD_CLKO** (100Mhz memory clk).

- TV output requires a 54Mhz crystal to drive **VO_CLK** (X1).
- Provision is made for an external **DAC_CLK** (CN10), **CORECLK** (CN13), & **SD_CLK** (CN7) to be used in preference to the above sources. (debug only).

2.5.2 Graphics DAC pins

The graphics DAC full-scale current can be controlled by adjusting the value of the **DAC_RSET** input resistors (R72 & R74) according to the following equation:-

$$\textbf{Rset (ohms)} = (K * 1000 * I_{VREF(v)}) / I_{OUT\ (mA)}$$

Where: K = scaling factor (please refer to NEC AAD38UOB, 2.5v, 220Mhz Megamacro Triple 8-bit video DAC document)

I_{VREF} = Voltage reference input current

I_{OUT} = DAC Output current

DAC_VREF is supplied by a LM385_1.2 voltage reference device (D8) - Its value should be 1.235V.

DAC power (**DAC_AVDD**) is 2.5v and is a filtered version of the main 2.5v source.

Header CN10 provides a connection point for an external **DAC_CLK** (debug only).

2.5.3 Video / TV output pins

The TV Output from PMX1 is available in either S-Video , composite video or RGBS. This AGP card design, however, will only support S-Video or composite video outputs - see TV out block for further details.

A 54Mhz (25ppm stability) crystal (X1) is required to drive **VO_CLK**.

A filtered version of the main 2.5v source is used to power the TV output block.

2.5.4 AGP interface pins

AGP interface complies with AGP v1.0 specification.

2.5.5 Video input interface pins

This consists of an 8-bit YUV data bus plus 1 clock and 3 strobe inputs. These signals can be driven by a Bt829a video decoder or MPEG-2 decoder via the VMI port.

An I^2C bus allows the video decoder to be controlled by PMX1.

2.5.6 PLL Power

The PLL analog power supply require a separately filtered source and good isolation from other power/gnd planes. Careful attention was paid to this during the PCB layout. PLL power is a filtered version of the main 2.5v source. The PLL ground path is at the same potential as digital ground although the two ground paths are physically isolated so as to prevent digital noise passing through the PLL ground plane.

2.5.7 Graphics Display Memory pins

Memory control lines (RAS#, CAS# etc.) have series termination resistors fitted to dampen signal slew-rate. These resistors are fitted close to the PMX1 chip. An option for fitting AC termination to the ends of the clock lines is also available. (see sheet 7).

The header (CN7) is for an alternative memory clock (**SD_CLK**) source.

Power-On Strapping Requirements

Graphics memory is accessed via a 64-bit data bus (SD_D<63:0>) which is also used for power-on initialisation of the configuration registers listed in table 2.1 below.

BIT	FUNCTION	FIT PULL-UP	FIT PULL-DWN	DEFAULT
SD_D<0>	AGP_ENABLE	ENABLE (R1)	DISABLE (R2)	DISABLED
SD_D<1>	VGA_ENABLE	ENABLE	DISABLE	JP1 LINK
SD_D<2>	EXT. DAC_CLK SELECT	EXT. CLK (R8)	INT. CLK (R11)	INT. CLK
SD_D<3>	EXT. CORECLK SELECT	EXT. CLK (R14)	INT. CLK (R20)	INT. CLK
SD_D<4>	VGA BIOS DECODE	ENABLE (R25)	DISABLE (R31)	DISABLED

Table 2-1 Power-on configuration

Register Description

AGP_Enable	- enable/disables AGP features
VGA_Enable	- enable/disables VGA core
DAC_clk select	- selects between external or internal DAC_clk
CORE_clk select	- selects between external or internal core clk
VGA BIOS DECODE	- allows decode of C1000 BIOS.

2.6 Sheet 6 - Memory Signal buffers

When large memory configurations (16Mb) are supported, an optional 16-bit latch (U4) and a clock buffer (U1) can be fitted to reduce the capacitive loading on the memory address and control lines. These can be removed when smaller configurations are supported.

2.7 Sheet 7 - SDRAM Display Memory

The following memory options are available for this card design:-

Memory Configuration	SDRAM Device	Circuit References
8Mb	4 x 16Mbit	U2 , U3, U7, U11
16Mb	8 x 16Mbit	U13 , U14, U15, U16

Table 2-2

2.8 Sheet 8 - Video Graphics Out

RGB signals are designed for 75 ohm doubly-terminated lines. A 75 ohm resistor connects each RGB line to 0V. This provides half of the necessary 37.5 ohm DC load - the other half is in the display monitor .Each RGB line has a double-pole LC filter network to control edge-rates and reduce EMC emissions. These filters are located close to the standard 15-pin output connector (CN6).

The routing of the RGB tracks was carefully considered due to the high edge-rates are present. Long parallel tracks were avoided and isolation from other signal tracks was maintained in an attempt to reduce cross-talk. Track impedance should be as close to 75 ohms as possible.

Overcurrent/overvoltage protection is provided by diodes D1-D7.

Hsync (HS) and Vsync (VS) lines are filtered by a 33R/120pf RC network.

DDC2B support is provided by the second I^2C bus from PMX1.

VGA output uses a standard 15-way, sub-miniature D-type connector (CN6).

2.9 Sheet 9 - TV output buffer

The TV out interface on this AGP card provides PAL /NTSC support for S-Video (YC) and composite video (CVBS) output.

Video op-amps (U8 -U9) are used to provide additional filtering and amplification. The op-amps are driven by a single +5V power supply.

TV output signals are referenced to analog ground (0VA). This ground plane is isolated especially from audio and digital grounds.

S-Video/composite video TV output is available through a 4-pin miniDIN connector which is on a separate card mounted on the rear of the main card. CN8 is the header which connects these two cards together.

Jumper (JP2) settings allows selection between S-Video and composite video output.

2.10 Sheet 10 - Power

This AGP reference card has the following power requirements:-

2.5V - (2.5Vdd) PMX1 core supply voltage.
Supplied by LT1580-2.5 regulator (U6)

3.3V - (3.3Vdd) PMX1 output buffers & memory & 2.5v regulator supply.
Supplied via AGP connector form motherboard

3.3V - (Vddq) Separate 3.3V for AGP buffers.
Supplied from the motherboard.

+ 5V - Video Op-amps, video decoder (daughter card) supply

+12V - Fan Supply - sourced from the motherboard.

3. Card Construction

This AGP adapter card has been designed as a 4 layer card with 2 signal layers, 1 split power plane (3.3v/5v) and 1 split ground plane (analogue grounds/digital grounds).

4. Mechanical details

The card is available as a AGP adapter card design for NLX form factor machines (also compatible with ATX form factor)

The I/O on the back-panel consists of the following connector:-

- Royal Blue 15-pin, sub-miniature D-type monitor connector

Additional I/O is mounted on a separate daughter card with the following connectors:

(This is a limitation of the NLX form factor for AGP cards.)

- 4 pin miniDIN S-Video/composite video output
- 4 pin miniDIN S-Video/composite video input
- 4 pin audio-out header - for connection to sound card if MPEG-2 decoder is used.

The following internal connectors will be provided as well:

- 26 pin Video input Port A header
- 40 pin VMI Host port socket

5. APPENDIX A - BUS INTERFACE CONNECTIONS (PCI/AGP)

Pin Name	PCI Function	AGP Function	Note
FRAME#	Cycle Frame	Not used	
IRDY#	Initiator Ready	New meaning	
TRDY#	Target Ready	New meaning	
STOP#	Stop	Not used by A.G.P.	
DEVSEL#	Device Select	Not used by A.G.P.	
IDSEL	Initialisation Dev Sel	Not used by A.G.P.	
REQ#	Request	Same as PCI	
GNT#	Grant	Same as PCI	
RST#	Reset	Same as PCI	
AD[31:00]	Multiplexed Address/Data	Same as PCI	
C/BE[3:0]#	Bus Command/Byte Enables	Slightly different meaning	
PAR	Parity	Not used by A.G.P.	
INTA#	Interrupt A	Same as PCI	
CLK	Clock	Same as PCI	
PIPE#		Pipelined	
SBA[7:0]		Sideband Address Port	
RBF#		Read Buffer Full	
ST[2:0]		Status	
AD_STB0		AD Bus Strobe 0	
AD_STB1		AD Bus Strobe 1	
SB_STB		Sideband Strobe	

6. APPENDIX B - VMI HOST PORT CONNECTIONS

CONNECTOR B (40 Pin Female Dual Row Receptacle, 0.100 in. centres)			
Pin #	**Signal Name**	**Pin #**	**Signal Name**
Z1	+12v	Y1	HD[0]
Z2	HD[1]	Y2	Ground
Z3	Ground	Y3	HD[2]
Z4	HD[3]	Y4	HD[4]
Z5	+5V	Y5	HD[5]
Z6	HD[6]	Y6	HD[7]
Z7	OSC	Y7	HA[0]
Z8	HA[1]	Y8	HA[2]
Z9	HA[3]	Y9	+5V
Z10	Ground	Y10	RESET#
Z11	CS#	Y11	Ground
Z12	RD#	Y12	WR#
Z13	+3.3V	Y13	READY
Z14	SCLK	Y14	INTREQ#
Z15	LRCK	Y15	PCMDATA
Z16	+5V	Y16	+3.3V
Z17	User-Defined	Y17	User-Defined
Z18	User-Defined	Y18	KEY
Z19	INSERT#	Y19	AUDIOL
Z20	AUDGND	Y20	AUDIOR

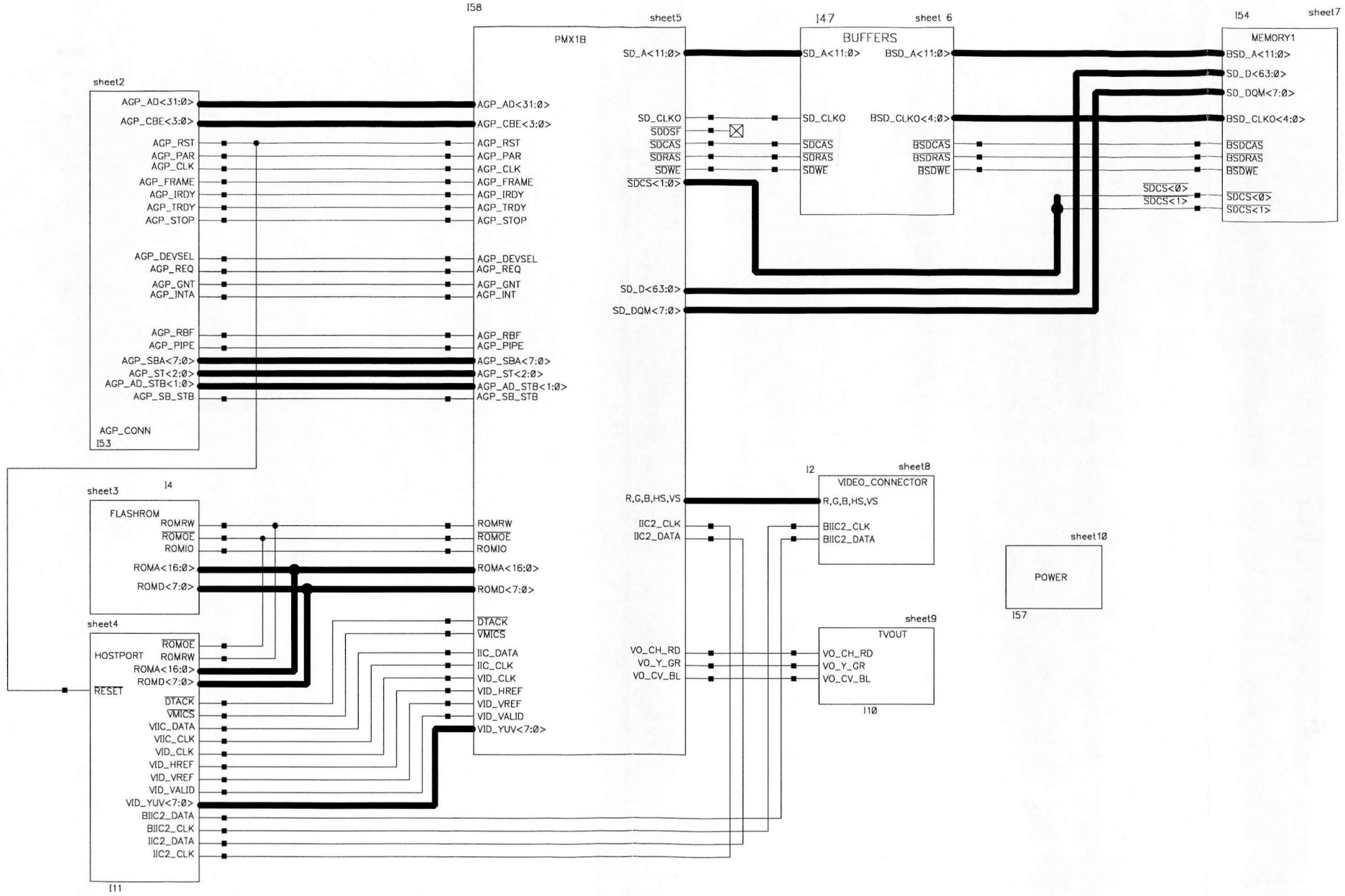
7. APPENDIX C - VIDEO PORT CONNECTIONS

CONNECTOR A (26 Pin Male Dual Row Header, 0.100 in. centres)					
Standard Feature Connector		**Video Port Implementation**		**Standard Feature Connector**	**Video Port Implementation**
Pin #	**Signal Name**	**Signal Name**	**Pin #**	**Signal Name**	**Signal Name**
Z1	Ground	0V	Y1	P0	VIDYUV[0]
Z2	Ground	0V	Y2	P1	VIDYUV[1]
Z3	Ground	0V	Y3	P2	VIDYUV[2]
Z4	EVIDEO#	VIDVALID	Y4	P3	VIDYUV[3]
Z5	ESYNC#	N/C	Y5	P4	VIDYUV[4]
Z6	EDCLK#	VIDVREF	Y6	P5	VIDYUV[5]
Z7	N/C	I2C_CLK	Y7	P6	VIDYUV[6]
Z8	Ground	0V	Y8	P7	VIDYUV[7]
Z9	Ground	0V	Y9	DCLK	VIDCLK
Z10	Ground	0V	Y10	BLANK#	VIDHREF
Z11	Ground	0V	Y11	HSYNC	N/C
Z12	N/C	N/C	Y12	VSYNC	N/C
Z13	N/C	I2C_DAT	Y13	Ground	0V

8. APPENDIX D - INDUSTRY REFERENCE SPECIFICATIONS

The following recognised specifications have been referred to in these design notes:-

- PCI Bus Specification v2.1
- Video Module Interface Specification v1.4
- Accelerated Graphics Port (AGP) Specification v1.0
- NLX form factor design guide.
- PMX1 Preliminary Data Sheet



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Drn: D.CHAPPELL | Date: 03/03/98 | Array Code: 00RV

VideoLogic
Home Park Estate,
Kings Langley, Herts.,
WD4 8LZ Tel 0923-260511

AGP Spec Notes:

Is IDSEL tied to AD16 internally or externally (ECR 22)
Vddq connects to AGP buffer on PMX chip
INTA# has been tied to AGP_INT, INTB# left unconnected. Is this OK?

This is 3.3v Vddq

VDD

+5V 3.3V

+12V

I129 A164

I132 A256

AGP_AD<31:0>

AGP_SBA<7:0>

AGP32BOT

AGP32TOP

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			B<5>	A<5>			
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AGP_CLK		I124 A286	B<7>	A<7>	I67 A11	AGP_RST	
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			B<41>	A<41>	I83 A301	AGP_FRAME	
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			B<43>	A<43>			
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I64 CN15

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Kings Langley, Herts
WD4 8LZ Tel 0923-2[illegible]511

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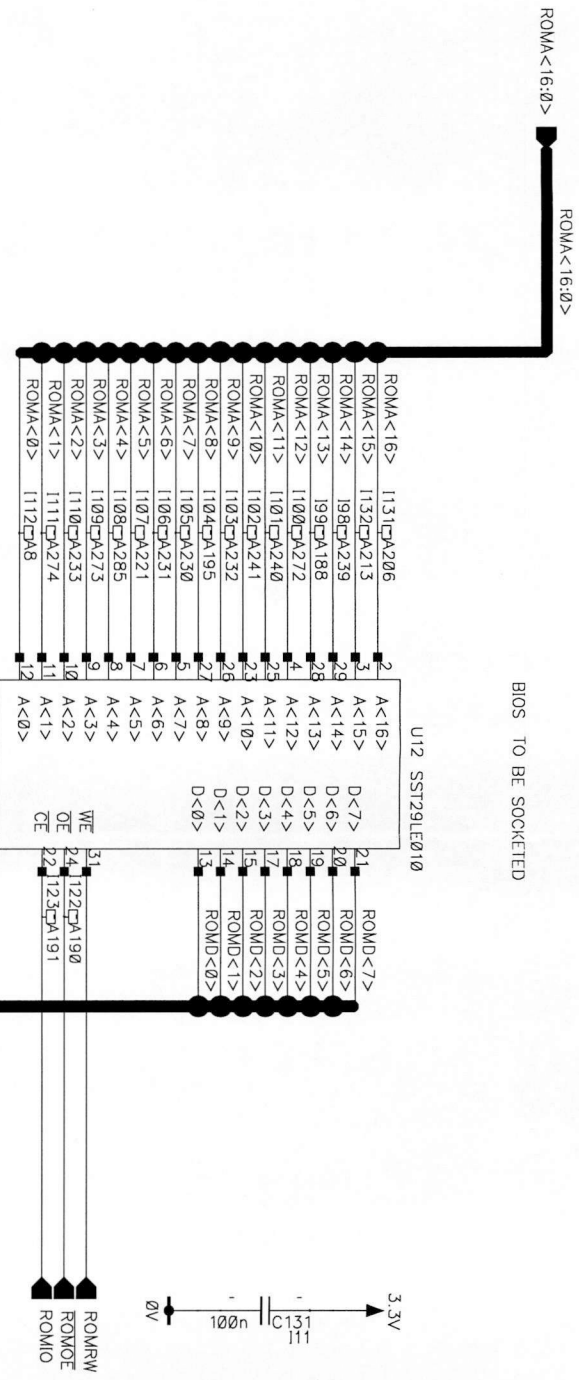

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+5V
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VID_YUV<7>
VID_CLK
VID_HREF
VID_VALID
VID_VREF
VIIC_CLK
VIIC_DATA
IIC2_DATA
IIC2_CLK
VID_YUV<7:0>
5v to 3v Conversion buffer
Only required for Bt829A
+5V
R24
NF0603
I204
BTOE
R30
NF0603
I208
ØV
For BT829 output enable control
Fit pull-down to enable
Fit pull-up to disable
Video In header
CN2 BDL-104-T-F
I210
AGND
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+5V 3.3V +12V
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CS I213□A27
DS
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ROMOE
VMICS
Avermedia Bt829a daughtercard
has incorrect VMI pin out.
Use configuration as shown
however R7 & R10 may need to
be swapped
R10
I171
NF0603
AVIDC
I189□A28
R7
I170
0
I188□A17
I90□A23
AVIDY I87□A10
AUDIOL I85□A15
AUDIOR I86□A12
I229
0
R78
Not required
for PMX1C
ØV
AGND
ØV
I230
0
R80
Not required
for PMX1C
ØV
Title: PMX1 AGP REFERENCE CARD - VMI PORT
Issue: Ø1
Sht No: 4
Array Code: ØØRV
Aprv:
Date: Ø3/Ø3/98
Engr: D.CHAPPELL
Drn: D.CHAPPELL
VideoLogic
Home Park Estate,
Kings Langley, Herts.,
WD4 8LZ Tel Ø923-26Ø511

U10

TBD_PMX1B

IQXO-14.31818 X2

IQXO_22A_54M X1

HF30ACB_453215 L8 / L5 / L9

Ext.Core Clk (debug) CN13

Ext.DAC Clk (debug) CN10

LM385M-1.2

25ppm part required

Additional decoupling

Power-on strapping

VGA_BIOS_HARD DECODE

EXT. DAC CLK SELECT

EXT. CORE CLK SELECT

EXT. MEMORY CLOCK CN7

VGA_ON_IN

VREF POT DIVIDER

PU/PD,s for Debug Only

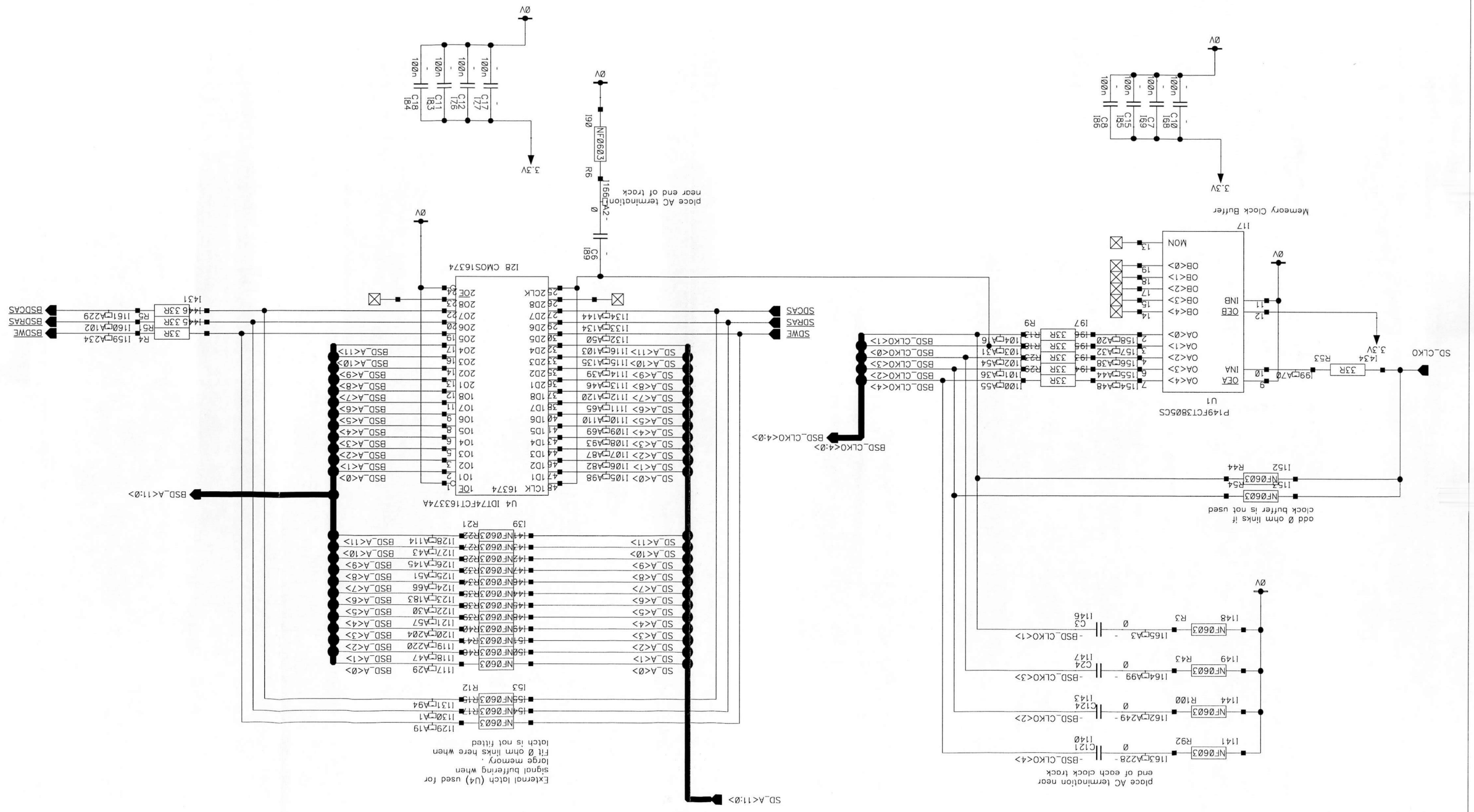
FOR AGP BOARD, 5V PINS CONNECTED TO AGP 3.3V

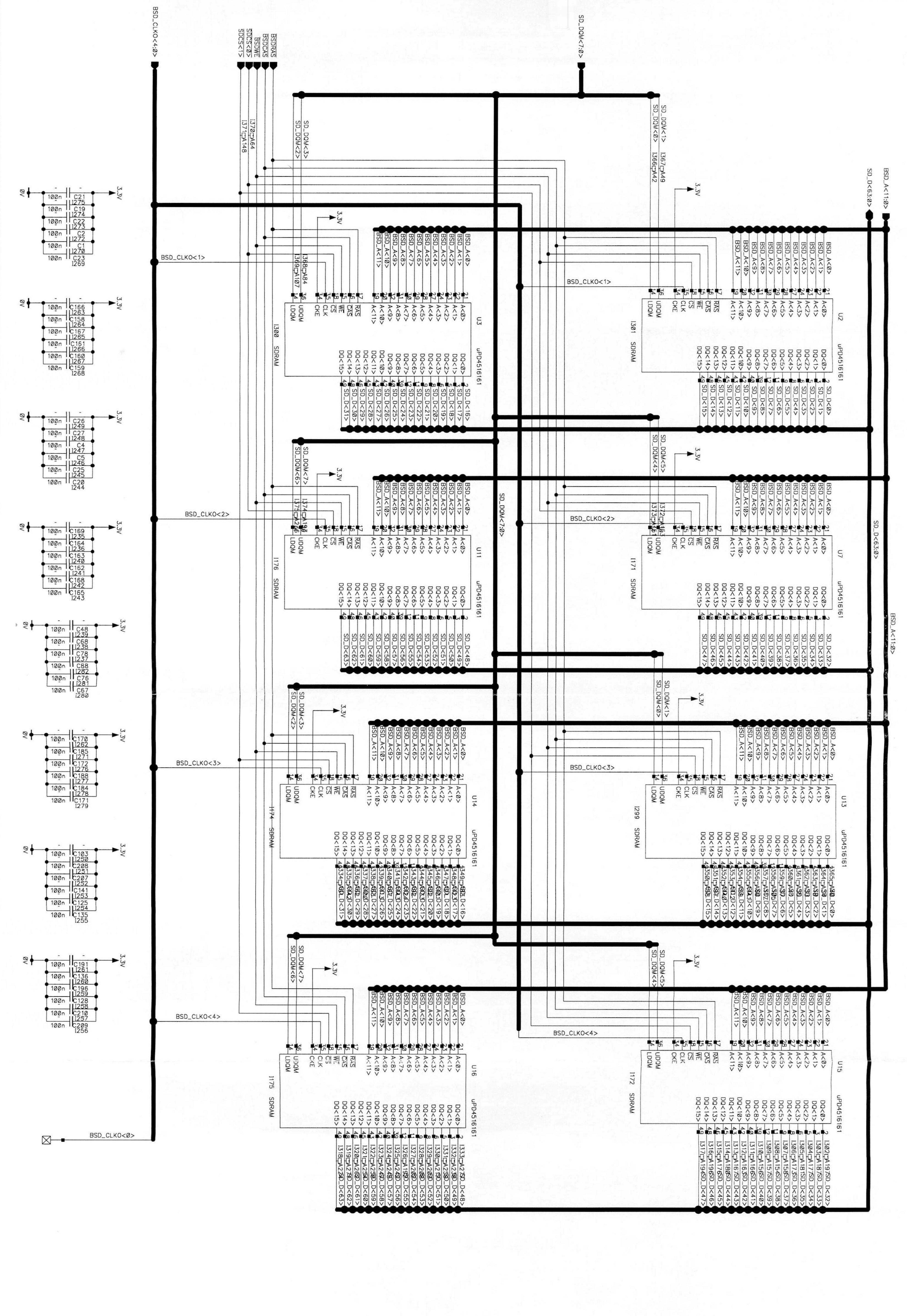
ANALOG GND SIGNALS:
ØVA0 – PLL AGND
ØVA1 – TV OUT AGND
ØVA2 – VIDEO IN AGND
ØVA3 – VGA AGND

VideoLogic	Home Park Estate, Ki… Langley, Herts., W… Z Tel Ø923–26Ø511	Title: PMX1 AGP REFERENCE CARD – PMX1 ASIC			
		Engr: D. CHAPPELL	Aprv:	Arr	Sht No: 5 / Issue: Ø1
		Drn: D.CHAPPELL	Date: Ø3/Ø3/97		

Videologic
Home Park Estate,
Kings Langley, Herts.,
WD4 8LZ Tel 0923-260511

Title:	PMX1 AGP REFERENCE CARD - SIGNAL BUFFERS
Engr: D.CHAPPELL	
Drn: D.CHAPPELL	
Aprv:	
Date: 03/03/98	
Array Code:	
00RV	
Sht No:	
6	
Issue:	
01	





VideoLogic — Home Park Estate, Kings Langley, Herts., WD4 8LZ Tel Ø923-26Ø511	Title: PMX1 AGP REFERENCE CARD – SDRAM GRAPHICS MEMORY				
	Engr: D.CHAPPELL	Aprv:	Array Code:	Sht No:	Issue:
	Drn: D.CHAPPELL	Date: Ø3/Ø3/98	ØØRV	7	Ø1

R,G,B,HS,VS

HS I105□A52 — 33R I89 R33 — I121□A95 — HSYN

VS I106□A53 — 33R I90 R26 — I114□A45 — VSYN

R I107□A178 — L7 I86 NL322522T_R10K — I112□A127 — L6 I79 MLF2012DR_15K — I115□A126

C57 I22 47p — ØVA3 — ØV

C66 I24 33p — ØVA3 — ØV

G I108□A115 — L4 I85 NL322522T_R10K — I111□A108 — L3 I82 MLF2012DR_15K — I116□A104

C29 I21 47p — ØVA3 — ØV

C54 I25 33p — ØVA3 — ØV

B I109□A85 — L2 I84 NL322522T_R10K — I110□A81 — L1 I83 MLF2012DR_15K — I117□A96

C16 I23 47p — ØVA3 — ØV

C28 I26 33p — ØVA3 — ØV

RED

GREEN

BLUE

I118□A68

I119□A56

481_443
CN6

I130□A168FUSE

I7

R62 I76 AXIALRXE_Ø17

R69 I77 SMDSMD_Ø5Ø_2

+5V

C9 I27 100p — ØV ØVA3

C13 I28 100p — ØV ØVA3

I92 Ø R16 — ØV ØVA3 — ØVEXT

+5V — R19 2K2 I87 — R36 2K2 I88

BIIC2_CLK

BIIC2_DATA

+5V

BAV99W D1 — D34

BAV99W D3 — D36

BAV99W D2 — D35

BAV99W D5 — D37

BAV99W D6 — D38

I131□A137 — D41 — D7 BAV99W

ØV ØVA3

Place diodes close
to video connector

PMX1 AGP REFERENCE CARD – VGA CONNECTOR

Engr: D. CHAPPELL	Aprv:	Date: 03/03/98	Array Code: ØØRV	Snt No: 8
Drn: D.CHAPPELL				Issue: 1

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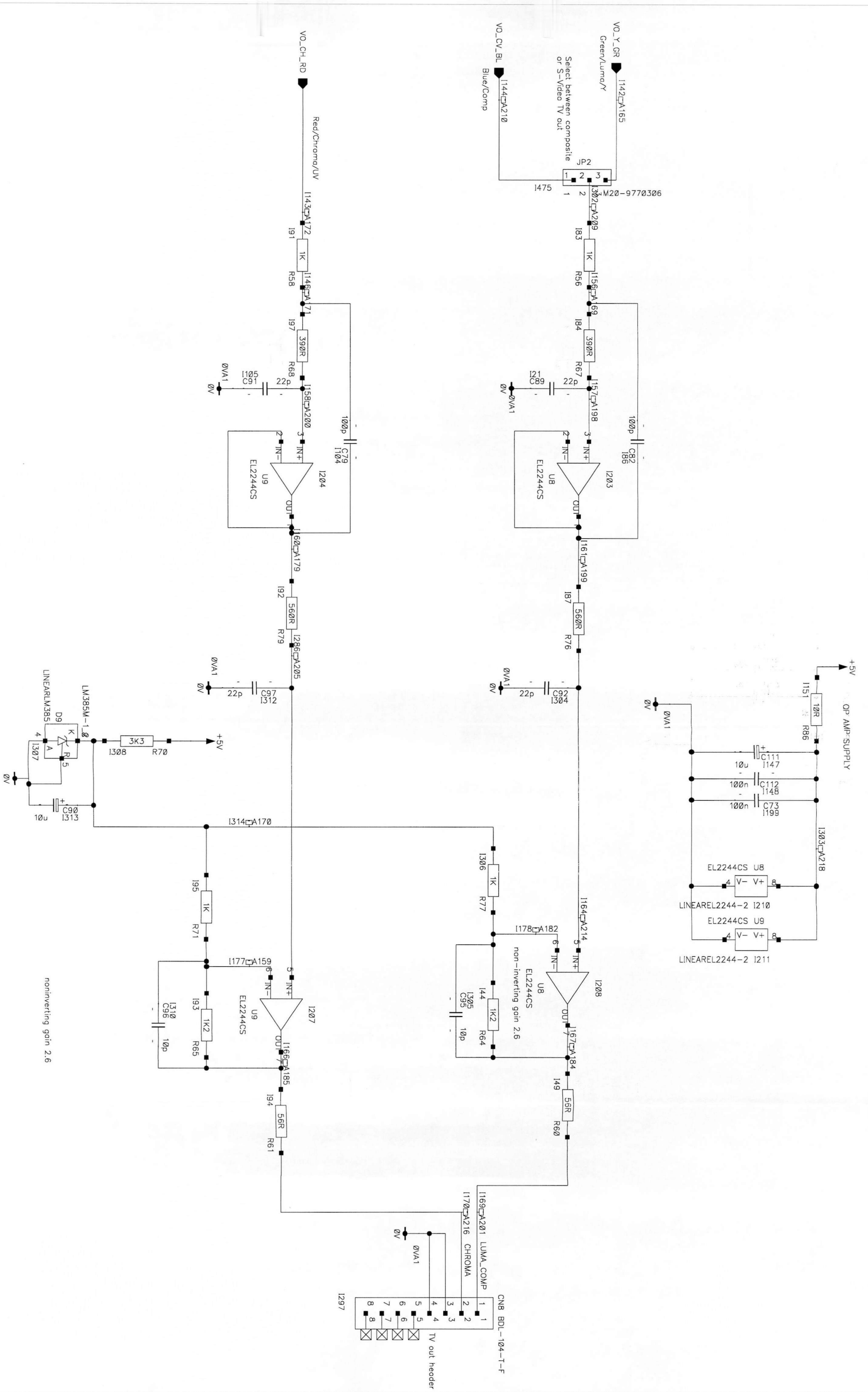
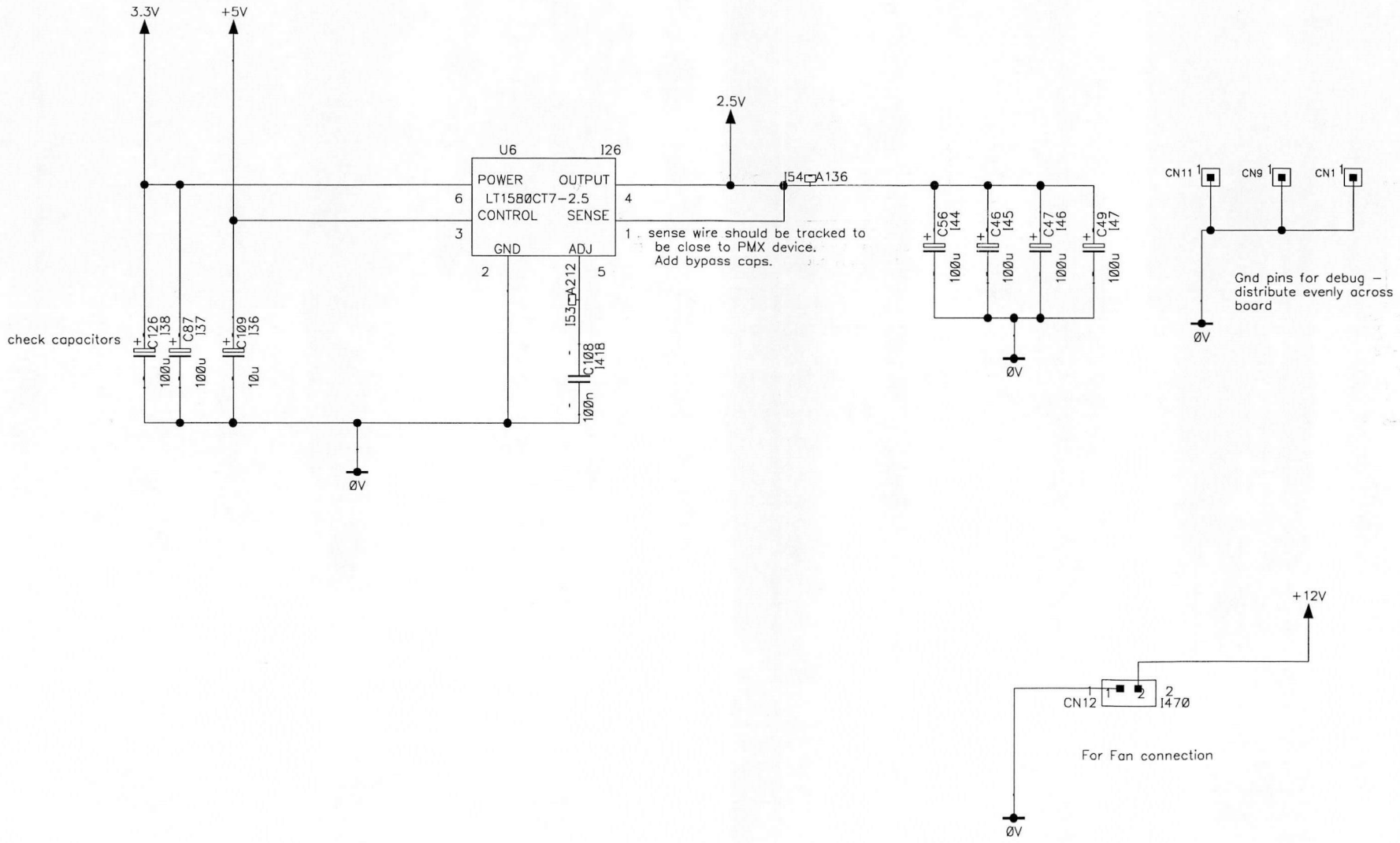
WD4 8LZ Tel Ø923–26Ø511

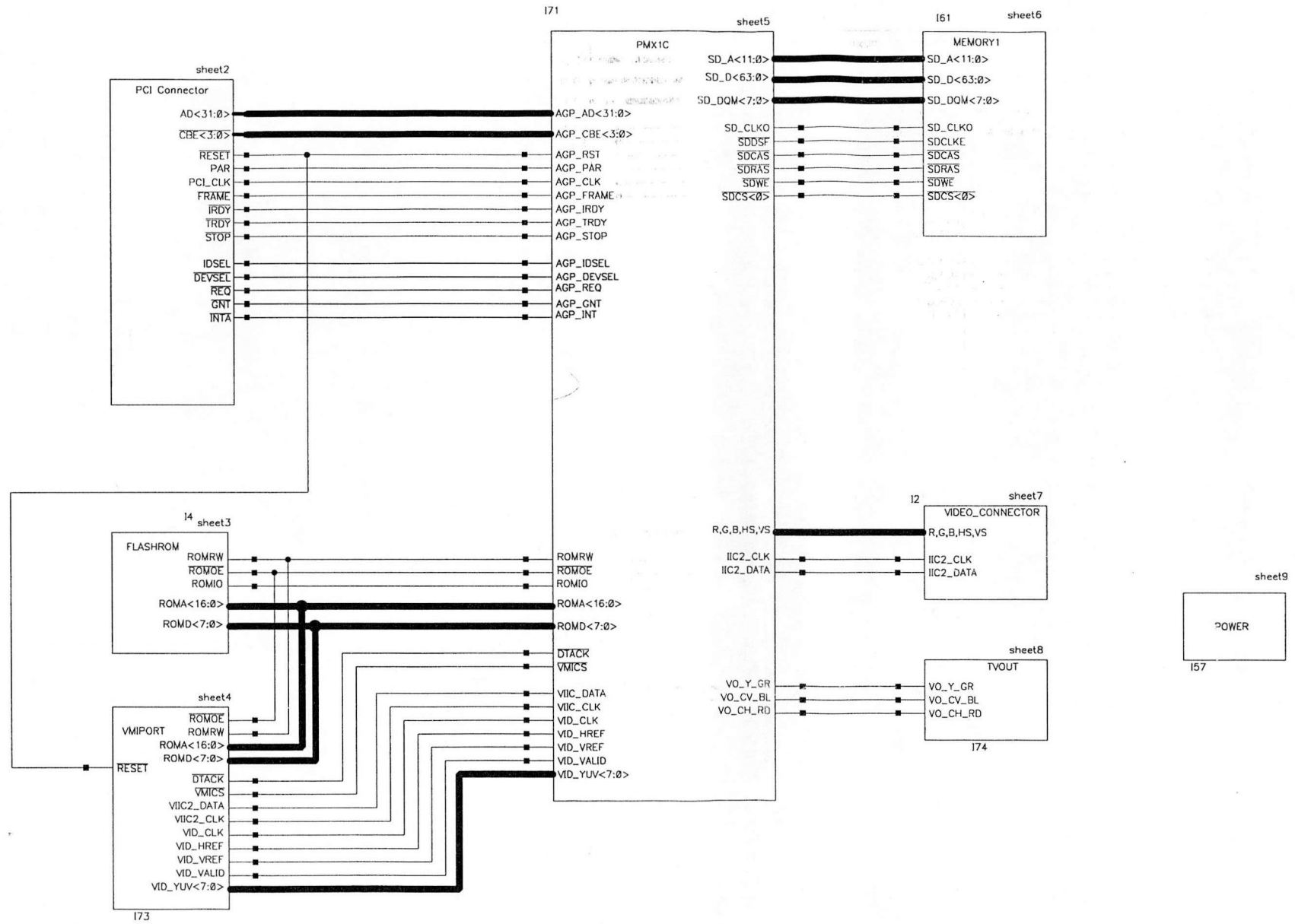


VideoLogic Home Park Estate, Kings Langley, Herts., WD4 8LZ Tel 0923-260511	Title: PMX1 AGP REFERENCE CARD – TV OUT BUFFER				
	Engr: D.CHAPPELL	Aprv:	Array Code:	Sht No:	Issue:
	Drn: D.CHAPPELL	Date: 03/03/98	00RV	9	01



Title: PMX1 AGP REFERENCE CARD – POWER REGS.			Issue:	Ø1
Engr: D.CHAPPELL	Aprv:	Assy Code:	Sht No:	10
Drn: D.CHAPPELL	Date: Ø3/Ø3/98	ØØRV		

VideoLogic
Home Park Estate,
Kings Langley, Herts.,
WD4 8LZ Tel Ø923–26Ø511



Title: PMX1 PCI REFERENCE CARD DESIGN – TOP LEVEL

Engr: D.CHAPPELL | Aprv: | Array Code: | Sht No: | Issue:

Drn: D.CHAPPELL | Date: 11/05/98 | ØØSO | 1 | draftA

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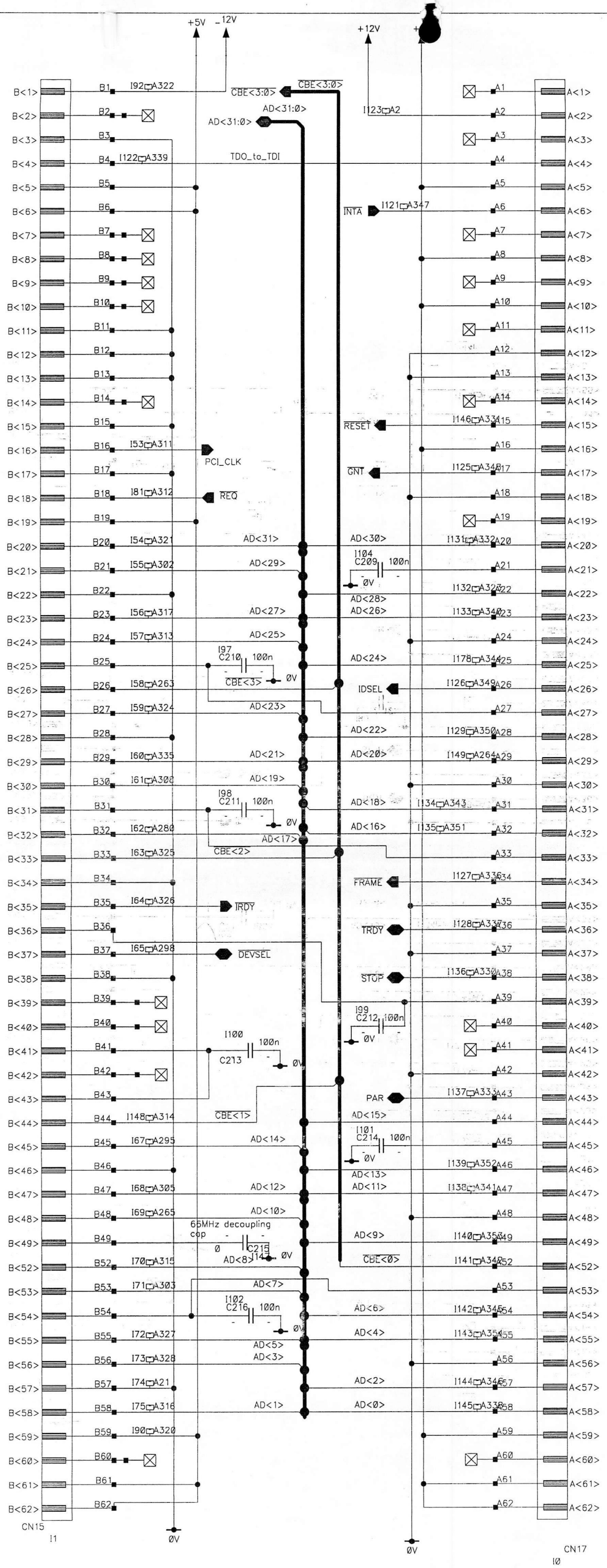
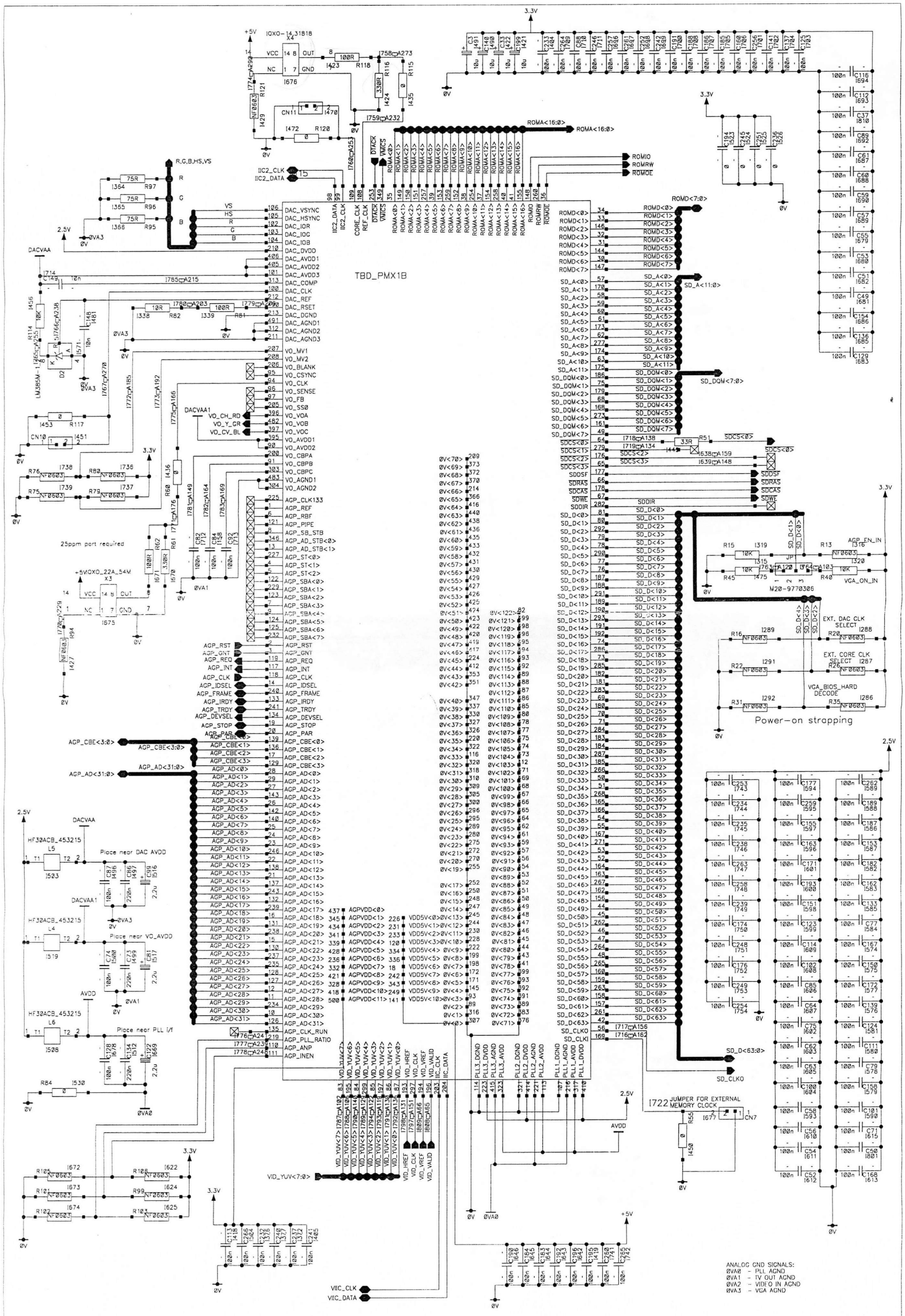
WD4 8LZ Tel Ø923-260511



VideoLogic Home Park Estate, Kings Langley, Herts., WD4 8LZ Tel 0923-260511	Title PMX1 PCI REFERENCE CARD – PCI CONNECTOR			
	Engr: D.CHAPPELL	Aprv:	Array Code:	Sht No:	Issue:
	Drn: D.CHAPPELL	Date: 10/05/98	0050	2	draft A



VideoLogic Home Park Estate, Kings Langley, Herts., WD4 8LZ Tel 0923-260511	Title: PMX1 PCI REFERENCE CARD – PMX1 ASIC				
	Engr: D. CHAPPELL	Aprv:	Array Code:	Sht No:	Issue:
	Drn: D.CHAPPLLL	Date: 03/03/98	005A	6	Draft A

版	記事	承認
1	新規作成 1998.10.23 秋口田	相場

ST-14438-01

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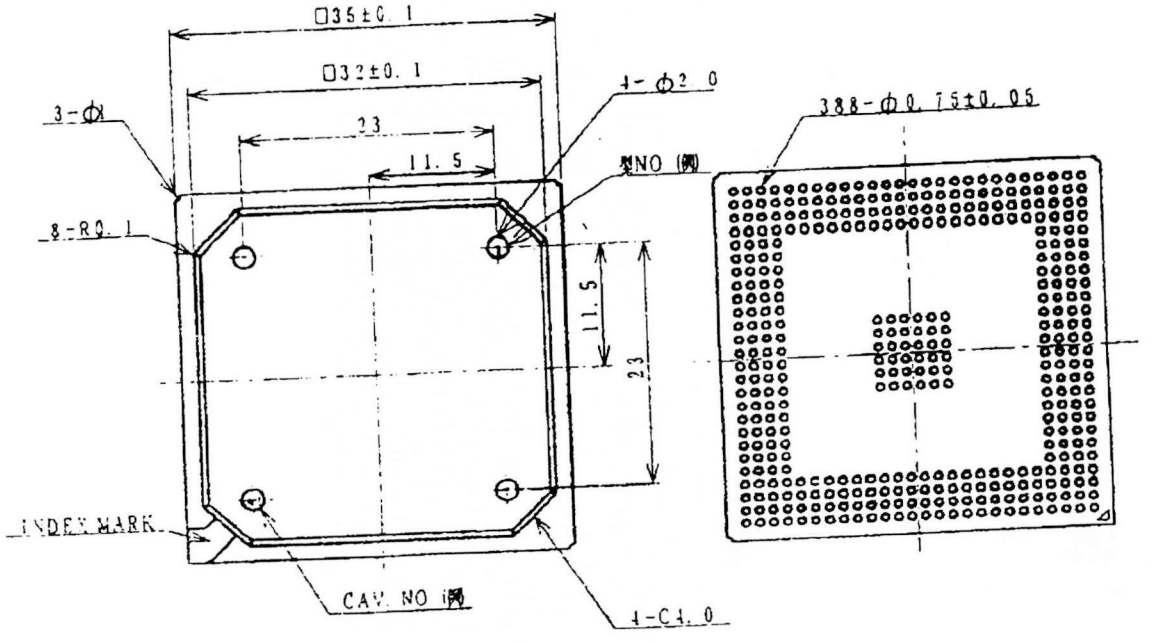
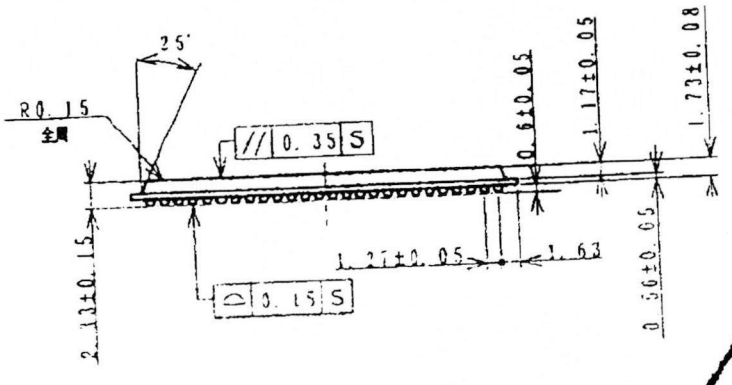
2	
3	
4	
5	





フィルム				仕様書
型 ROM				組立図
整理期限	素材名	所要寸度	仕上および処理	部品表
	特に指定のないものは普通公差	第三角法	R度 1.5/1	
整理番号	設計 秋口田 / 檜口	査閲	承認 相場	388pin PBGA (□35) PKG設計図

ST-14438-01

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